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(54) LAYERED CAPACITOR, WIRING BOARD, DECOUPLING CIRCUIT AND HIGH FREQUENCY CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the equivalent series inductance (ESL) of a layered capacitor.
SOLUTION: First and second through conductors 20, 21, by which a first internal electrode 14 and a second internal electrode 15 which are faced with each other and a first external terminal electrode and a second external terminal electrode are connected electrically, are arranged in such a way that magnetic fields induced by currents flowing in the internal electrodes 14, 15 are offset mutually. The arrangement pitch of the through conductors 20, 21 is designated as P (unit: mm). The total number of the through holes 20, 21 is designated as N. Then, P/N<=0.085 is set.

CLAIMS

[Claim(s)]
[Claim 1]Have a capacitor body containing two or more dielectric layers laminated, and inside said capacitor body, At least one pair of 1st and 2nd internal electrodes of a quadrangle which counters mutually via said specific dielectric layer are provided, On at least one [which is prolonged in said internal electrode and parallel of said capacitor body] principal surface, They are provided by the 1st and 2nd outer terminal electrodes, and inside said capacitor body, Two or more 1st penetration conductors that penetrate said specific dielectric layer so that said 1st internal electrode and said 1st outer terminal electrode may electrically be connected in the state where it was electrically insulated to said 2nd internal electrode, And two or more 2nd penetration conductors that penetrate said specific dielectric layer so that said 2nd internal electrode and said 2nd outer terminal electrode may electrically be connected in the state where it was electrically insulated to said 1st internal electrode are formed, respectively, Said two or more 1st and 2nd penetration conductors are formed so that it may be distributed over the whole region of said 1st and 2nd internal electrodes, and said 1st penetration conductor and said 2nd penetration conductor, It is arranged so that a magnetic field induced by current which flows through said internal electrode may be offset mutually, and so that each other may be mutually adjoined with a distribution state substantially located at each square vertex, A multilayer capacitor chosen in an array pitch of said 1st and 2nd penetration conductors so that P/N may become 0.085 or less when the total number of P (a unit is mm) and said 1st and 2nd penetration conductors is set to N.
[Claim 2]The multilayer capacitor according to claim 1 chosen so that said P/N may become 0.04 or less.
[Claim 3]The multilayer capacitor according to claim 1 or 2 formed so that said 1st and 2nd outer terminal electrodes may be distributed over punctiform in relation to each of said 1st and 2nd penetration conductors, respectively.

[Claim 4]The multilayer capacitor according to claim 3 with which a solder bump is formed in said 1st and 2nd outer terminal electrodes.
[Claim 5]The multilayer capacitor according to any one of claims 1 to 4 with which said 1st and 2nd outer terminal electrodes are provided only on said one principal surface.
[Claim 6]Said 1st and 2nd outer terminal electrodes are the multilayer capacitors of said two principal surfaces according to any one of claims 1 to 4 currently formed upwards respectively.
[Claim 7]The multilayer capacitor according to any one of claims 1 to 4 with which said 1st outer terminal electrode is formed on said one principal surface, and said 2nd outer terminal electrode is formed on said principal surface of another side.
[Claim 8]The multilayer capacitor according to any one of claims 1 to 7 used as a decoupling capacitor connected to a power supply circuit for an MPU chip with which a microprocessing unit is equipped.
[Claim 9]A wiring board in which the multilayer capacitor according to any one of claims 1 to 8 was mounted.
[Claim 10]An MPU chip with which a microprocessing unit is equipped is carried, It has a hot side wiring conductor for power supplies and a grounded wiring conductor for supplying a power supply for said MPU chip, The wiring board according to claim 9 by which one side of said 1st and 2nd outer terminal electrodes of said multilayer capacitor is electrically connected to a hot side wiring conductor for said power supplies, and another side of said 1st and 2nd outer terminal electrodes is connected to said grounded wiring conductor.

[Claim 11]The wiring board according to claim 9 or 10 to which said 1st and 2nd outer terminal electrodes are connected by a vamp.
[Claim 12]A decoupling circuit provided with the multilayer capacitor according to any one of claims 1 to 8.
[Claim 13]A high frequency circuit provided with the multilayer capacitor according to any one of claims 1 to 8.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]In this invention, it is related with a multilayer capacitor, a wiring board, a decoupling circuit, and a high frequency circuit.
Therefore, it is related with the wiring board, decoupling circuit, and high frequency circuit which are constituted using the multilayer capacitor which may be especially applied advantageously in a high frequency circuit, and this multilayer capacitor.

[0002]
[Description of the Prior Art]From the former a certain most typical multilayer capacitor, . For example, have two or more pairs of 1st and 2nd internal electrodes arranged by turns in the laminating direction of a dielectric layer while countering mutually via a specific dielectric layer so that it may consist of ceramic dielectrics and two or more dielectric layers laminated and two or more capacitor units may be formed. It has the capacitor body. The 1st and 2nd outer terminal electrodes are formed in the 1st and 2nd end faces of a capacitor body, respectively. The 1st internal electrode is prolonged even on the 1st [of a capacitor body] end face, and is electrically connected to the 1st outer terminal electrode here, and the 2nd internal electrode is prolonged even on the 2nd end face, and is electrically connected to the 2nd outer terminal electrode here.
[0003]In this multilayer capacitor, the current which flows into the 1st outer terminal electrode from the 2nd outer terminal electrode, It flows into the 2nd internal electrode from the 2nd outer terminal electrode, it results and ranks second to the 1st internal electrode through a dielectric layer from this 2nd internal electrode, and results to the 1st outer terminal electrode through the inside of this 1st internal electrode.
[0004]The equivalent circuit of a capacitor is expressed in the circuit where CLR was connected in series, when [at which resistance of the electrode was mainly set to R] calling the capacity of a capacitor C and calling equivalent in-series inductance (ESL) L and equivalent series resistance (ESR).
[0005]In this equivalent circuit, resonance frequency (f0) is f0=1/. [2pix(LxC) 1/2] It stops functioning as a capacitor in frequency higher than a next door and resonance frequency. If in other words L, i.e., an ESL value, is small, resonance frequency (f0) becomes high and can be used more by high frequency. Although using copper for an internal electrode and making ESR small etc. is considered, in order to use in a microwave range, the capacitor by which low ESL-ization was attained is needed.
[0006]Low ESL-ization is called for also in the capacitor used as a decoupling capacitor connected to the MPU chip of microprocessing units (MPU), such as a workstation and a personal computer, in the power supply circuit which supplies a power supply.
[0007]Drawing 8 is a block diagram showing schematically an example of the connection configuration about MPU1 and the power supply section 2 which

mentioned above.
[0008]MPU1 is provided with MPU chip 3 and the memory 4 with reference to drawing 8. It is for the power supply section 2 supplying a power supply to MPU chip 3, and the decoupling capacitor 5 is connected to the power supply circuit from the power supply section 2 to MPU chip 3. The signal circuit comprises MPU chip 3 at the memory 4 side.
[0009]In the case of the decoupling capacitor 5 used in relation to MPU1 which was mentioned above as well as the usual decoupling capacitor, are used for smoothing to noise absorption or change of a power supply, but. These days in MPU chip 3, that to which the clock frequency amounts even to 1 GHz exceeding 500 MHz is planned, If it is in the use as which high-speed operation is required in relation to such MPU chip 3, the function (function which supplies electric power among several nanoseconds from quantity of electricity charged by the capacitor when the electric power at the time of a standup, etc. is required for urgency) as a quick power supply is required.
[0010]For this reason, even if it is in the decoupling capacitor 3 in MPU1, an inductance component is low as much as possible, for example, it is needed that they are 10 or less pH, and realization of the capacitor with an inductance value low in this way is desired.
[0011]if it explains more concretely -- a certain MPU chip 3 -- about [DC] -- 2.0V is supplied -- power consumption -- about -- it is the design into which the current like 24W, i.e., 12A, flows. While MPU1 is not operating for the reduction of the power consumption, the specification from which power consumption is dropped on less than 1W is adopted as a sleep mode. Electric power required for an active mode needs to be supplied to the inside of the number clock of operations at MPU chip 3 at the time of the conversion to an active mode from a sleep mode. In the time of the conversion to an active mode from a sleep mode, it is necessary to supply electric power between the time of 4 to 7 nanoseconds in the clock frequency of 500 MHz.
[0012]However, since supplying above-mentioned electric power does not meet the deadline from the power supply section 2, supplying a power supply to MPU chip 3 is performed by discharging the electric charge charged by the decoupling capacitor 5 put on time until it supplies a power supply from the power supply section 2, and about three MPU chip.
[0013]If it is in some whose operation clock frequency is 1 GHz, in order to satisfy such a function, it is needed that ESL of the about three-MPU chip decoupling capacitor 5 is at least 10 or less pH.
[0014]
[Problem(s) to be Solved by the Invention]ESL of the common multilayer capacitor described previously is about 500-800 pH, and is far from 10 or less pH which was mentioned above. Thus, an inductance component is brought about in a multilayer capacitor because the magnetic flux it is decided that that direction will be is induced, it originates in this magnetic flux and a self-inductance ingredient arises by the direction of the current which flows in a multilayer capacitor.

[0015]The structure of a multilayer capacitor where low ESL-ization can be attained under a background which was mentioned above, For example, it is proposed in JP,2-256216,A, U.S. Pat. No. 5880925, JP,2-159008,A, JP,11-144996,A, JP,7-201651,A, etc.
[0016]In order to base above-mentioned low ESL-ization mainly on offset of the magnetic flux induced in a multilayer capacitor and to make it offset of such magnetic flux arise, diversifying the direction of the current which flows in a multilayer capacitor is performed. And while increasing the number of the cash-drawer portions of the internal electrode pulled out so that it may electrically be connected to this by increasing the number of the terminal electrodes formed on the outside surface of a capacitor body for diversification of the direction of this current, Turning the drawer portion of an internal electrode in some directions is performed.
[0017]However, the measure for the reduction in ESL in the multilayer capacitor

proposed that it mentioned above is still insufficient in the point of an effect.

[0018]For example, although the structure which pulls out an internal electrode even on two sides in which a capacitor body counters is indicated by JP,2-256216,A, U.S. Pat. No. 5880925, and JP,2-159008,A, It is surmised that low ESL-ization can be attained only to about 100 pH.
[0019]Although the structure which pulls out an internal electrode on four sides of a capacitor body is indicated by JP,11-144996,A, 40pH is only indicated as a most outstanding ESL value.
[0020]Although the structure which pulls out an internal electrode even to the principal surface of the upper and lower sides of a capacitor body is indicated by JP,7-201651,A, 50pH is only indicated as a most outstanding ESL value.

[0021]Therefore, in the high frequency circuit (a power source line is included) for MPU chips where such a multilayer capacitor is used, in order to realize ESL of 10 or less pH conventionally, for example, mounting in a wiring board as a state which connected two or more multilayer capacitors in parallel is performed. As a result, the packaging area for a multilayer capacitor becomes large, and has become a cause which checks the miniaturization of the electric appliance which constitutes such a high frequency circuit.
[0022]Then, the purpose of this invention is to provide the multilayer capacitor improved so that low ESL-ization could be attained more effectively.

[0023]Other purposes of this invention are to provide the wiring board, decoupling circuit, and high frequency circuit which are constituted using a multilayer capacitor which was mentioned above.
[0024]
[Means for Solving the Problem]A multilayer capacitor concerning this invention is provided with a capacitor body containing two or more dielectric layers laminated.
[0025]At least one pair of 1st and 2nd internal electrodes of a quadrangle which counters an inside of this capacitor body mutually via a specific dielectric layer are provided, and the 1st and 2nd outer terminal electrodes are provided on at least one [which is prolonged in an internal electrode and parallel of a capacitor body] principal surface.
[0026]Two or more 1st penetration conductors that penetrate a specific dielectric layer so that the 1st internal electrode and 1st outer terminal electrode may electrically be further connected to an inside of a capacitor body in the state where it was electrically insulated to the 2nd internal electrode, And two or more 2nd penetration conductors that penetrate a specific dielectric layer so that the 2nd internal electrode and 2nd outer terminal electrode may electrically be connected in the state where it was electrically insulated to the 1st internal electrode are formed, respectively.
[0027]Two or more 1st and 2nd penetration conductors mentioned above are formed so that it may be distributed over the whole region of the 1st and 2nd internal electrodes.
[0028]These 1st and 2nd penetration conductors are arranged so that a magnetic field induced by current which flows through an internal electrode may be offset mutually, and so that each other may be mutually adjoined with a distribution state substantially located at each square vertex.
[0029]And in order to solve technical SUBJECT mentioned above, it is characterized by choosing an array pitch of said 1st and 2nd penetration conductors so that P/N may become 0.085 or less when the total number of P (a unit is mm) and said 1st and 2nd penetration conductors is set to N.

[0030]Preferably, P/N mentioned above is chosen so that it may become 0.04 or less.
[0031]As for the 1st and 2nd outer terminal electrodes, in a multilayer capacitor concerning this invention, it is preferred to be provided, respectively so that

it may be distributed over punctiform in relation to each of the 1st and 2nd penetration conductors.
[0032]In an above-mentioned case, to the 1st and 2nd outer terminal electrodes, it is preferred that a solder bump is formed.
[0033]As for the 1st and 2nd outer terminal electrodes, in a multilayer capacitor concerning this invention, it is preferred to be provided only on one principal surface of a capacitor body. even if the 1st and 2nd outer terminal electrodes are formed on each of the two principal surfaces of a capacitor body, the 1st outer terminal electrode may be formed on one principal surface, and the 2nd outer terminal electrode may be formed on the principal surface of another side.

[0034]A multilayer capacitor concerning this invention is advantageously used as a decoupling capacitor connected to a power supply circuit for an MPU chip with which MPU is equipped.
[0035]This invention is turned also to a wiring board in which a multilayer capacitor which was mentioned above was mounted again.
[0036]As mentioned above, when this invention is turned to a wiring board, in that one concrete embodiment. An MPU chip with which a microprocessing unit is equipped is carried in this wiring board, and a wiring board, It has a hot side wiring conductor for power supplies and a grounded wiring conductor for supplying a power supply for an MPU chip, One side of the 1st and 2nd outer terminal electrodes of a multilayer capacitor is electrically connected to a hot side wiring conductor for power supplies, and another side of the 1st and 2nd outer terminal electrodes is connected to a grounded wiring conductor.
[0037]In a wiring board mentioned above, the 1st and 2nd outer terminal electrodes with which a multilayer capacitor is equipped are preferably connected by a vamp.
[0038]This invention is turned also to a decoupling circuit further provided with a multilayer capacitor which was mentioned above.
[0039]This invention is turned also to a high frequency circuit provided with a multilayer capacitor which was mentioned above.
[0040]
[Embodiment of the Invention]Drawing 1 and drawing 2 show the multilayer capacitor 11 by a 1st embodiment of this invention. Here, drawing 1 is a top view showing the internal structure of the multilayer capacitor 11, and (1) and (2) show a mutually different section. Drawing 2 is a sectional view in alignment with line II-II of drawing 1.
[0041]The multilayer capacitor 11 is provided with the capacitor body 13 containing two or more dielectric layers 12 laminated. The dielectric layer 12 comprises a ceramic dielectric, for example.
[0042]At least one pair of 1st and 2nd internal electrodes 14 and 15 of the quadrangle which counters the inside of the capacitor body 13 mutually via the specific dielectric layer 12 are formed. According to this embodiment, the 1st and 2nd internal electrodes 14 and 15 make a square, and two or more pairs of 1st and 2nd internal electrodes 14 and 15 are formed.
[0043]Even if there is little principal surface 16 and 17 which extends in parallel with the internal electrodes 14 and 15 of the capacitor body 13, on the other hand by this embodiment, the 1st and 2nd outer terminal electrodes 18 and 19 are formed on one principal surface 17.
[0044]The 1st and 2nd outer terminal electrodes 18 and 19 are formed on the principal surface 17, respectively so that it may be distributed over punctiform in relation to each of the 1st and 2nd penetration conductors 20 and 21. According to this embodiment, the 1st and 2nd outer terminal electrodes 18 and 19 are provided with the solder bumps 24 and 25 formed the electric conduction pads 22 and 23 and on them, respectively.
[0045]Two or more 1st penetration conductors 20 that penetrate the specific dielectric layer 12 so that the 1st internal electrode 14 and 1st outer terminal electrode 18 may electrically be further connected to the inside of the capacitor body 13 in the state where it was electrically insulated to the 2nd internal

electrode 15 are formed. Two or more 2nd penetration conductors 21 that penetrate the specific dielectric layer 12 so that the 2nd internal electrode 15 and 2nd outer terminal electrode 19 may electrically be connected in the state where it was electrically insulated to the 1st internal electrode 14 are formed.

[0046]Two or more 1st and 2nd penetration conductors 20 and 21 mentioned above are formed so that it may be distributed over the whole region of the 1st and 2nd internal electrodes 14 and 15.
[0047]In this embodiment, two or more 1st and 2nd internal electrodes 14 and 15 are formed respectively, The electric capacity to which multiple connection of the electric capacity formed between the 1st and 2nd internal electrodes 14 and 15 was carried out, and multiple connection was carried out in this way by the 1st and 2nd penetration conductors 20 and 21 is taken out between the 1st and 2nd outer terminal electrodes 18 and 19.
[0048]The 1st penetration conductor 20 mentioned above and the 2nd penetration conductor 21 are arranged so that the magnetic field induced by the current which flows through the internal electrodes 14 and 15 may be offset mutually. The 1st penetration conductor 20 and 2nd penetration conductor 21 are arranged so that each other may be mutually adjoined with the distribution state substantially located at each square vertex.
[0049]It is chosen so that P/N may become 0.085 or less as characteristic composition of this invention, when the total number of P (a unit is mm) and the 1st and 2nd penetration conductors 20 and 21 is set [array pitch / of the 1st and 2nd penetration conductors 20 and 21] to N, and preferably, it is chosen so that it may become 0.04 or less.
[0050]For example, in [if the specific multilayer capacitor 11 shown in drawing 1 is explained] this multilayer capacitor 11, Since the total number N of the 1st and 2nd penetration conductors 20 and 21 is 5x5=25 and it is referred to as P/N<=0.085, array-pitch P, It is chosen so that it may become 0.085x25 mm or less, i.e., 2.215 mm, and preferably, since it is referred to as P/N<=0.04, array-pitch P is chosen so that it may become 0.04x25 mm or less, i.e., 1 mm.

[0051]Therefore, when array-pitch P is 2.215 mm or less 2 mm, a length of one side of the total number N is the 1st and 2nd penetration conductors 20 and 21 of 5x5=25, for example 2x(5-1) =8 When it explains from another viewpoint which can be arranged to the internal electrodes 14 and 15 of the square of [mm] and the 1st and 2nd internal electrodes 14 and 15 are the squares of 8 mm x 8 mm, for example, by a distribution state as shown in drawing 1. If the total number N arranges the 1st and 2nd penetration conductors 20 and 21 of 5x5=25, array-pitch P will be 8/4=2. [mm] About a next door and P/N, it is set to 2/25=0.08, and the conditions of P/N<=0.085 can be fulfilled.
[0052]The conditions about such P/N are searched for by the experiment conducted in order to check the effect of the reduction in ESL. Below, this experiment is explained.
[0053]On the basis of the composition with which the multilayer capacitor 11 as shown in A drawing 1 and drawing 2 is equipped, while, In each sample which set the size of the principal surfaces 16 and 17 of the capacitor body 13 to 2.5 mm x 2.5 mm, 4.5 mm x 4.5 mm, and 10 mm x 10 mm, respectively, while changing the total number N of the penetration conductors 20 and 21, ESL was calculated about what changed array-pitch P according to it. ESL was calculated from the self-resonant frequency obtained by measuring a frequency characteristic by the network analyzer.
[0054]The sizes of the principal surface of a capacitor body are 2.5 mm x 2.5 mm, and the relation between P/N when the total number N of a penetration conductor and array-pitch P are changed, and ESL is shown in the following table 1 in the multilayer capacitor whose sizes of an internal electrode are 2.0 mm x 2.0 mm.

[0055]
[Table 1]

試料番号	貫通導体		P／N	ESL (pH)
	合計数(N)	配列ピッチ(P) (mm)		
1	5×5	0.5	0.020	9.30
2	4×4	0.67	0.042	23.4
*3	3×3	1.0	0.111	66.9
*4	2×2	2.0	0.500	300

[0056]The sizes of the principal surface of a capacitor body are 4.5 mm x 4.5 mm, and the relation between P/N when the total number N of a penetration conductor and array-pitch P are changed, and ESL is shown in the following table 2 in the multilayer capacitor whose sizes of an internal electrode are 4.0 mm x 4.0 mm.

[0057]
[Table 2]

試料番号	貫通導体		P／N	ESL (pH)
	合計数(N)	配列ピッチ(P) (mm)		
5	6×6	0.8	0.022	9.10
6	5×5	1.0	0.040	15.4
7	4×4	1.33	0.083	28.2
*8	3×3	2.0	0.222	81.4
*9	2×2	4.0	1.000	408

[0058]The sizes of the principal surface of a capacitor body are 10 mm x 10 mm, and the relation between P/N when the total number N of a penetration conductor and array-pitch P are changed, and ESL is shown in the following table 3 in the multilayer capacitor whose sizes of an internal electrode are 8 mm x 8 mm.

[0059]
[Table 3]

試料番号	貫通導体		P／N	ESL (pH)
	合計数(N)	配列ピッチ(P) (mm)		
10	6×6	1.6	0.044	12.4
11	5×5	2.0	0.080	22.4
*12	4×4	2.67	0.167	49.2
*13	3×3	4.0	0.444	140
*14	2×2	8.0	2.000	643

[0060]In Table 1 thru/or 3, it is the sample besides the scope of this invention which gave * to the sample number.
[0061]If Table 1 thru/or 3 is referred to, it cannot be concerned with the size of an internal electrode, but specific correlation can be found out between P/N and ESL.
[0062]That is, according to the samples 1, 2, 5-7, 10, and 11 which are P/N<=0.085, and 15-17, ESL of 30 or less pH can be attained. In particular, in the case of P/N<=0.04, ESL of 16 or less pH can be attained like the samples 1, 5, and 6.
[0063]Thus, when ESL can be made low, for example, it is referred to as P/N<=0.022 like the samples 1 and 5 so that P/N is small, ESL of 10 or less pH can be attained.
[0064]In the embodiment described above, although the 1st and 2nd internal electrodes 14 and 15 were making the square, the shape of these internal electrodes 14 and 15 may be a rectangle.
[0065]Drawing 3 is a figure equivalent to drawing 1 (1) showing the multilayer capacitor 26 by a 2nd embodiment of this invention. In the multilayer capacitor 26 shown in drawing 3, the internal electrodes 14 and 15 are making the rectangle as mentioned above. In drawing 3, the same reference mark is given to the element equivalent to the element shown in drawing 1, and the overlapping explanation is

omitted to it.
[0066]As mentioned above, the 1st and 2nd internal electrodes 14 and 15 (in drawing 3) that make a rectangle The graphic display of the 2nd internal electrode 15 is omitted. On the basis of the composition of the multilayer capacitor 26 which it has, while, ESL when the total number N of the penetration conductors 20 and 21 and array-pitch P were changed was calculated by the same method as the case of Table 1 thru/or 3.
[0067]The sizes of the principal surface of a capacitor body are 2.5 mm x 4.5 mm, and the relation between P/N when the total number N of a penetration conductor and array-pitch P are changed, and ESL is shown in the following table 4 in the multilayer capacitor whose sizes of an internal electrode are 2.0 mm x 4.0 mm.

[0068]
[Table 4]

試料番号	貫通導体		P／N	ESL (pH)
	合計数(N)	配列ピッチ(P) (mm)		
15	5×9	0.5	0.011	5.72
16	4×7	0.67	0.024	12.7
17	3×5	1.0	0.067	29.4
*18	2×3	2.0	0.333	170

[0069]In Table 4, it is the sample besides the scope of this invention which gave * to the sample number.
[0070]As shown in Table 4, even if it is a case where an internal electrode is a rectangle, specific correlation has appeared between P/N and ESL. And like the case where it is shown in Table 1 thru/or 3, like the samples 15-17, when referred to as P/N<=0.085, ESL of 30 or less pH can be attained. In the case of P/N<=0.04, more specifically, 16 or less pH of ESL(s) of 12.7 or less pH can be attained like the samples 15 and 16.
[0071]ESL can be made lower, and when P/N is set to 0.011, very low ESL called 5.72pH can be attained like the sample 15, so that P/N is small, even if it is a case where an internal electrode is a rectangle.
[0072]As shown in drawing 1 or drawing 3, by these embodiments, the 1st penetration conductor 20 and 2nd penetration conductor 21 are arranged so that each other may be mutually adjoined with the distribution state substantially located at each square vertex. The square which specifies such a distribution state may not necessarily be an exact square geometrically. This is explained referring to drawing 4.
[0073]In drawing 4, the square 27 which some of 1st and 2nd penetration conductors 20 and 21 are illustrated, and specifies the distribution state of these penetration conductors 20 and 21 is illustrated.
[0074]In such a square 27, about the each length P1 of the 1st and 2nd adjacent neighborhoods 28 and 29, i.e., the array pitch of the neighborhood 28 direction of the 1st, and the array pitch P2 of the neighborhood 29 direction of the 2nd, Not only the case of P1=P2 but the thing which fulfills the conditions of P1-/P2<1.2 when referred to as P1>P2, for example is substantially made into the square in this specification. In the case of P1-/P2 >=1.2, the magnetic flux generated in an internal electrode cannot be offset effectively, and sufficient low ESL-ization cannot be attained to it.
[0075]Drawing 5 is a figure equivalent to drawing 2 showing the multilayer capacitor 30 by a 3rd embodiment of this invention. In drawing 5, the same reference mark is given to the element equivalent to the element shown in drawing 2, and the overlapping explanation is omitted to it.
[0076]In the multilayer capacitor 30 shown in drawing 5, the 1st outer terminal electrode 18 is formed on one principal surface 16 of the capacitor body 13, and it is characterized by forming the 2nd outer terminal electrode 19 on the principal surface 17 of another side.
[0077]Drawing 6 is a figure equivalent to drawing 2 showing the multilayer

capacitor 31 by a 4th embodiment of this invention. In drawing 6, the same reference mark is given to the element equivalent to the element shown in drawing 2, and the overlapping explanation is omitted to it.
[0078]In the multilayer capacitor 31 shown in drawing 6, the both sides of the 1st and 2nd outer terminal electrodes 18 and 19 are characterized by the thing of the two principal surfaces 16 and 17 of the capacitor body 13 established upwards respectively.
[0079]If it is in the multilayer capacitor 11 shown in drawing 2, the flow of the current on the section shown in drawing 2 in the 1st penetration conductor 20 and 2nd penetration conductor 21 can be mutually turned to an opposite direction. On the other hand, if it is in the multilayer capacitor 31 shown in the multilayer capacitor 30 shown in drawing 5, and drawing 6, the current which flows in the 1st penetration conductor 20 and 2nd penetration conductor 21 becomes mutual in the same direction. From this, it can be said about the effect over the reduction in ESL that the multilayer capacitor 11 shown in drawing 2 is more excellent.

[0080]as mentioned above, about the number of internal electrodes or the number of outer terminal electrodes, and the number of penetration conductors, although the multilayer capacitor concerning this invention was explained in relation to illustrated various embodiments, as long as the conditions about P/N mentioned above are fulfilled, it can change into versatility. About the sectional shape of a penetration conductor, it may be changed into a quadrangle, a hexagon, etc. not only in a round shape like a graphic display, for example.
[0081]The multilayer capacitor concerning this invention can be advantageously used as the decoupling capacitor 5 with which MPU1 shown in above-mentioned drawing 8 is equipped, for example. Thus, the structure of MPU which uses the multilayer capacitor concerning this invention as a decoupling capacitor is explained below according to the constructional example shown in drawing 7.

[0082]MPU33 is provided with the wiring board 35 of the multilayer structure by which the cavity 34 was formed in the undersurface side with reference to drawing 7. The surface mount of MPU chip 36 is carried out to the upper surface of the wiring board 35. In the cavity 34 of the wiring board 35, the multilayer capacitor 11 concerning this invention which functions as a decoupling capacitor, for example, the multilayer capacitor concerning a 1st embodiment, is accommodated. The surface mount of the wiring board 35 is carried out on the mother board 37.
[0083]The surface and inside the wiring board 35, the required wiring conductor is formed in MPU33, and connection as shown in drawing 8 is attained with these wiring conductors so that it may be illustrated roughly.
[0084]Explanation of a typical thing forms the hot lateral electrode 38 for power supplies, and the ground electrode 39 in the inside of the wiring board 35.

[0085]The hot lateral electrode 38 for power supplies via the hot side beerhole conductor 40 for power supplies, It is electrically connected to the 1st outer terminal electrode 18 of the multilayer capacitor 11, and via the hot side beerhole conductor 41 for power supplies, It is electrically connected to the specific terminal 42 of MPU chip 36, and is electrically further connected to the hot side electric conduction land 44 of the mother board 37 via the hot side beerhole conductor 43 for power supplies.
[0086]The ground electrode 39 via the beerhole conductor 45 for grounds, It is electrically connected to the 2nd outer terminal electrode 19 of the multilayer capacitor 11, and via the beerhole conductor 46 for grounds, It is electrically connected to the specific terminal 47 of MPU chip 36, and is electrically further connected to the ground side electric conduction land 49 of the mother board 37 via the beerhole conductor 48 for grounds.
[0087]Although not illustrated in detail in drawing 7, connection by a vamp is applied to connection with the 1st and 2nd outer terminal electrodes 18 and 19 of the multilayer capacitor 11 and the beerhole conductors 40 and 45 which were

mentioned above.
[0088]In drawing 7, the graphic display of the memory equivalent to the memory 4 shown in drawing 8 is omitted.
[0089]
[Effect of the Invention]As mentioned above, according to the multilayer capacitor concerning this invention, inside the capacitor body containing two or more dielectric layers laminated. At least one pair of 1st and 2nd internal electrodes that counter mutually via a specific dielectric layer are provided, On at least one [which is prolonged in an internal electrode and parallel of this capacitor body] principal surface, They are provided by the 1st and 2nd outer terminal electrodes, and inside a capacitor body, Two or more 1st penetration conductors that electrically connect the 1st internal electrode and 1st exterior electrodes, And two or more 2nd penetration conductors that electrically connect the 2nd internal electrode and 2nd outer terminal electrode are formed, respectively, Since the 1st and 2nd penetration conductors are arranged so that the magnetic field induced by the current which flows through an internal electrode may be offset mutually, First, in this point, since the current which flows into a multilayer capacitor can be turned in the various directions and current length can be shortened, ESL can be made small.
[0090]Not only it but two or more 1st and 2nd penetration conductors, Are provided so that it may be distributed over the whole region of the 1st and 2nd internal electrodes, and the 1st penetration conductor and 2nd penetration conductor, When the total number of P (a unit is mm) and the 1st and 2nd penetration conductors is set to N for the array pitch of the 1st and 2nd penetration conductors, having been arranged so that each other may be mutually adjoined with the distribution state substantially located at each square vertex, Making an array pitch small, since it is chosen so that P/N may become 0.085 or less, the number of penetration conductors will be increased and it becomes possible to attain much more low ESL-ization certainly.
[0091]Thus, in this invention, since the range of effective P/N is clarified in order to attain low ESL-ization, it becomes easy to perform the optimal design to a multilayer capacitor for the reduction in ESL.
[0092]According to this invention, from low ESL-ization being attained as mentioned above. According to the multilayer capacitor which can high-frequency-ize resonance frequency of a multilayer capacitor, can high-frequency-ize the frequency area where a multilayer capacitor functions as a capacitor, and is applied to this invention. It can respond to high frequency-ization of an electronic circuit enough, for example, can use advantageously as the bypass capacitor in a high frequency circuit, or a decoupling capacitor.
[0093]If it is in the decoupling capacitor used combining with an MPU chip etc., the function as a quick power supply is required, but since ESL is low, even if the multilayer capacitor concerning this invention is turned to such a use, it can respond to high-speed operation enough.
[0094]The outer terminal electrode which it has in the multilayer capacitor concerning this invention makes it possible to apply bump connection advantageously, when it mounts a multilayer capacitor on a proper wiring board. In a present, for example, an MPU chip, semiconductor chip, although clock frequency follows on high-frequency-izing and it is in the tendency for bump connection to be used abundantly, existence of a principal surface terminal electrode suits this tendency. Such bump connection can make high density assembly possible, and can also suppress generating of the parasitic inductances in connection.
[0095]In this invention, each following embodiment raises more offset of magnetic flux which was mentioned above, or shortens current length more, and is effective by reduction of ESL.
[0096]It is chosen as the 1st so that P/N mentioned above may become 0.04 or less.
[0097]It is that the 1st and 2nd outer terminal electrodes are formed only on one

principal surface of a capacitor body the 2nd.

DESCRIPTION OF DRAWINGS

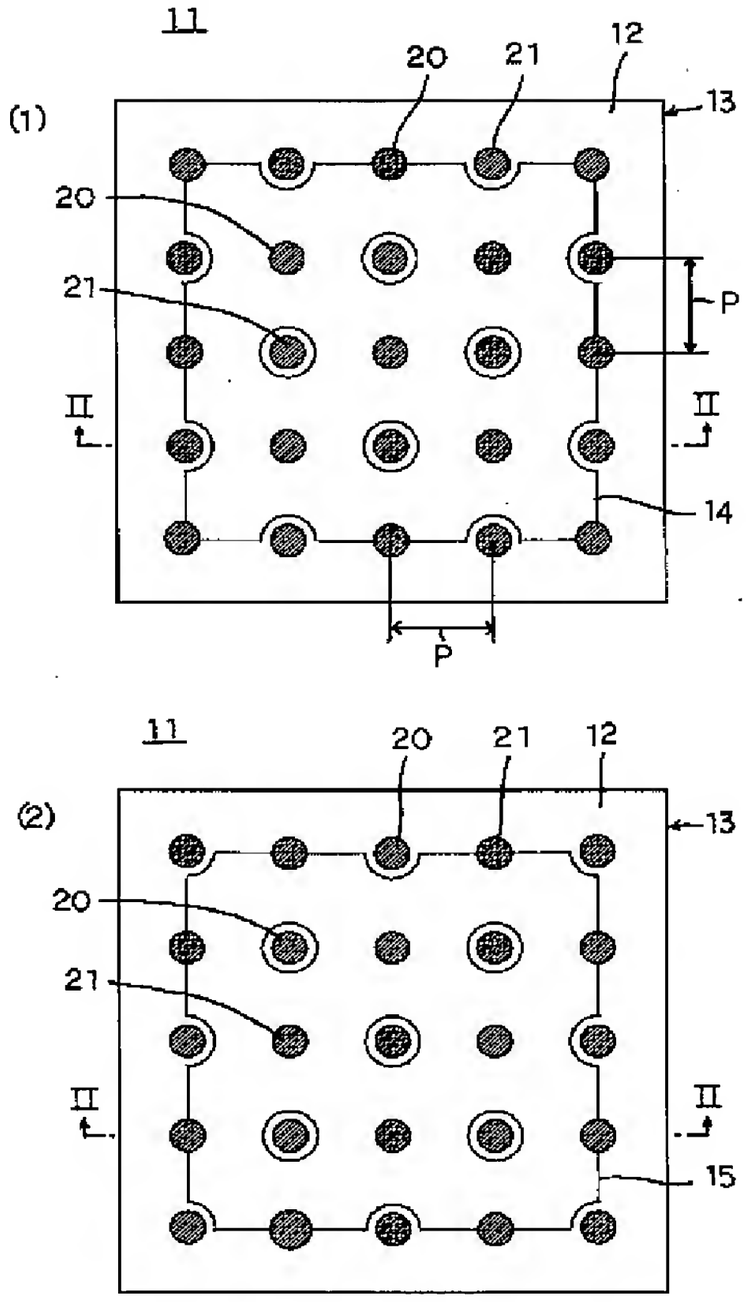
[Brief Description of the Drawings]
[Drawing 1]It is a top view showing the internal structure of the multilayer capacitor 11 by a 1st embodiment of this invention, and (1) shows the section along which the 1st internal electrode 14 passes, and, as for (2), it shows the section along which the 2nd internal electrode 15 passes.
[Drawing 2]It is a sectional view in alignment with line II-II of drawing 1.

[Drawing 3]It is a figure equivalent to drawing 1 (1) showing the multilayer capacitor 26 by a 2nd embodiment of this invention.
[Drawing 4]It is a figure for explaining the tolerance level about the difference of the array pitches P1 and P2 of the direction in alignment with each of the 1st and 2nd neighborhoods 28 and 29 that the square 27 which specifies the distribution state of the 1st and 2nd penetration conductors 20 and 21 adjoins.

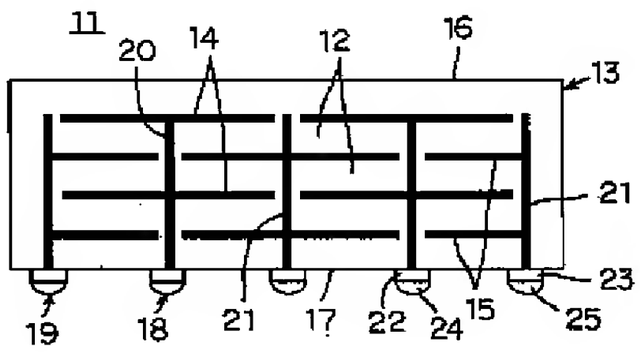
[Drawing 5]It is a figure equivalent to drawing 2 showing the multilayer capacitor 30 by a 3rd embodiment of this invention.
[Drawing 6]It is a figure equivalent to drawing 2 showing the multilayer capacitor 31 by a 4th embodiment of this invention.
[Drawing 7]It is a sectional view showing schematically the constructional example of MPU33 which uses the multilayer capacitor 11 by a 1st embodiment of this invention as a decoupling capacitor.
[Drawing 8]It is a block diagram showing schematically the connection configuration about MPU1 and the power supply section 2 interesting for this invention.
[Description of Notations]
1,33 MPU
2 Power supply section
3, 36 MPU chips
5 Decoupling capacitor
11, 26, 30, 31 multilayer capacitors
12 Dielectric layer
13 Capacitor body
14 The 1st internal electrode
15 The 2nd internal electrode
16 and 17 Principal surface
18 The 1st outer terminal electrode
19 The 2nd outer terminal electrode
20 The 1st penetration conductor
21 The 2nd penetration conductor
24, 25 solder bumps
27 Square
35 Wiring board
38 The hot lateral electrode for power supplies
39 Ground electrode
40, 41, and 43 Hot side beerhole conductor for power supplies
45, 46, and 48 Beerhole conductor for grounds
P, P1, P2 array pitch

DRAWINGS

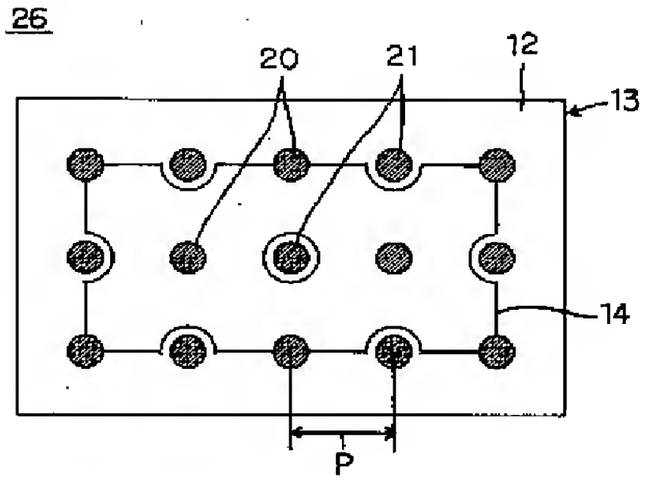
[Drawing 1]



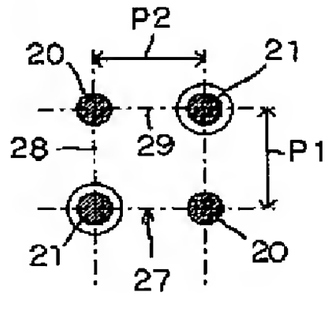
[Drawing 2]



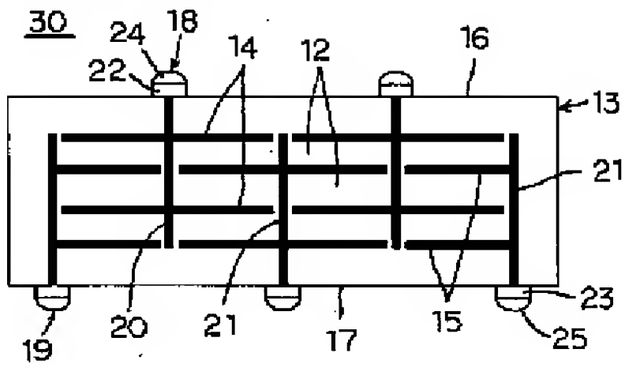
[Drawing 3]



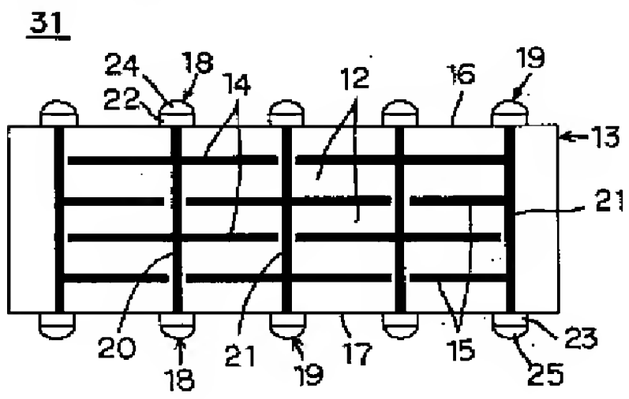
[Drawing 4]



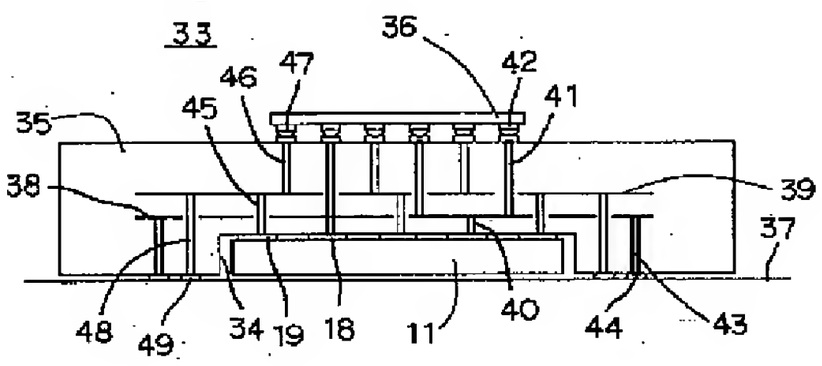
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Drawing 8]